IN THE CLAIMS:

1. (Amended) A built-in self-test controller, comprising:

a built-in self-test engine ~~capable of executing~~ configured to execute a built-in self-test and generating an indication of whether the executed built-in self-test is completed; and a built-in self-test signature including the indication, wherein the built-in self-test engine includes a logic built-in self-test engine and the built-in self-test signature includes a logic built-in self-test signature, and wherein the built-in self-test controller is configured to:

enter a reset state;

enter an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

scan a scan chain responsive to entering the initiate state;

step to a new scan chain; and

repeat the previous scanning and stepping until the content of a pattern generator in the logic built-in self-test engine of the built-in self-test controller equals a predetermined vector count.

2. (Cancelled).

3. (Amended) The built-in self-test controller of claim ~~2~~ 1, wherein the logic built-in self-test engine comprises:

a logic built-in self-test state machine; and

a pattern generator.

4. (Cancelled).

5. (Original) The built-in self-test controller of claim 1, wherein the logic built-in self-test signature comprises the content of a multiple input signature register.

6. (Amended) The built-in self-test controller of claim 1, wherein the built-in self-test engine ~~is~~ includes a memory built-in self-test engine and the built-in self-test signature ~~is~~ includes a memory built-in self-test signature.

7. (Cancelled).

8. (Amended) The built-in self-test controller of claim 6, wherein the memory built-in ~~selftest~~ self-test signature includes a bit indicating whether a memory built-in self-test is done.

9. (Amended) The built-in self-test controller of claim 6, wherein the memory built-in ~~selftest~~ self-test engine comprises:

a memory built-in self-test state machine; and

a nested memory built-in self-test engine operating the memory built-in self-test state machine.

10. (Amended) The built-in self-test controller of claim 9, wherein the memory built-in ~~selftest~~ self-test state machine ~~comprises~~ is configured to:

enter a reset state entered upon receipt of an external reset signal;

enter an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

enter a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state;

enter a test state entered into from the flush state; and

enter a done state entered into upon completing the test of each of a plurality of memory components in the memory built-in self-test.

11. (Amended) The built-in self-test controller of claim 9, wherein the memory built-in ~~selftest~~ self-test engine comprises:

a plurality of alternative memory built-in self-test state machines; and

a nested memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines.

12. (Amended) The built-in self-test controller of claim 11, wherein each of the memory ~~builtin~~ built-in self-test engines ~~comprises~~ is configured to:

enter a reset state entered upon receipt of an external reset signal;

enter an initiate state entered from the reset state upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

enter a flush state entered from the initiate state upon the initialization of components and signals in the memory built-in self-test domain in the initiate state; a test state entered into from the flush state; and

enter a done state entered into upon completing the test of each of a plurality of memory components in the memory built-in self-test.

13. (Cancelled).

14. (Cancelled).

15. (Cancelled).

16. (Cancelled).

17. (Amended) An integrated circuit device, comprising:

a plurality of memory components;

a logic core;

a testing interface; and

a built-in self-test controller, including:

a memory built-in self-test engine ~~capable of executing~~ configured to execute a built-in self-test on one of the memory components and the logic core and storing the results thereof, wherein the results

include an indication of whether an executed ~~builtin~~ built-in self-test is completed; and

a memory built-in self-test signature register capable of storing the results of an executed built-in self-test, including the indication;

and wherein the built-in self-test controller includes a logic built-in self-test engine configured to:

enter a reset state;

enter an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

scan a scan chain responsive to entering the initiate state;

step to a new scan chain; and

repeat the previous scanning and stepping until the content of a pattern generator in the logic built-in self-test engine of the built-in self-test controller equals a predetermined vector count.

18. (Amended) The integrated circuit device of claim 17, wherein the ~~built-in self-test engine is a~~ logic built-in self-test engine ~~and the register is~~ includes a multiple input signature register.

19. (Cancelled).

20. (Original) The integrated circuit device of claim 17, wherein the memory components include a static random access memory device.

21. (Original) The integrated circuit device of claim 17, wherein testing interface comprises a Joint Test Action Group tap controller.

22. (Amended) A method for performing a built-in self-test, the method comprising:

performing a built-in self-test, wherein performing the built-in self-test includes performing a logic built-in self-test including:

resetting a logic built-in self-test engine;

initiating a plurality of components and signals in a built-in self-test controller upon receipt of a logic built-in self-test run signal;

scanning a scan chain upon the initialization of the components and the signals;

stepping to a new scan chain;

repeating the previous scanning and stepping until the content of a pattern generator in a logic built-in self-test engine of the built-in self-test controller equals a predetermined vector count;

generating an indication of whether the logic built-in self-test is completed; and

storing the indication, wherein storing the indication includes setting a bit in a multiple input signature register.

~~including generating a indication of whether the builtin~~ built-in ~~self-test is completed; and~~

~~storing the indication.~~

23. (Cancelled).

24. (Cancelled).

25. (Amended) The method of claim ~~23~~ 22, further comprising at least one of:

setting a bit in the multiple input signature register indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.

26. (Original) The method of claim 22, wherein performing the built-in self-test includes performing a memory built-in self-test and storing the indication includes setting a bit in a memory built-in self-test signature register.

27. (Original) The method of claim 26, wherein performing the memory built-in self-test includes:

resetting a memory built-in self-test engine;

initiating a plurality of components and signals in a built-in self-test controller upon receipt of at least one of a memory built-in self-test run signal and a memory built-in self-test select signal;

flushing the contents of a plurality of memory components to a known state after initialization of the components and the signals; and testing the flushed memory components.

28. (Amended) The method of claim 26, wherein performing the memory built-in self-test further includes ~~at least one of:~~

storing the results of the memory built-in self-test in the memory built-in self-test signature register~~; and~~

~~storing the results of at least one paranoid check in the memory built-in self-test signature register~~.

29. (Cancelled).

30. (Cancelled).

31. (Cancelled).

32. (Cancelled).